S34ML04G3 Internal ECC Corrections and Status

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Associated Part Family: S34ML04G3

This application note, AN223237, details the internal ECC engine features used in the design of SkyHigh 1X-nm S34ML04G3 and offer special commands to enable the user to monitor the internal ECC correction activities and status.

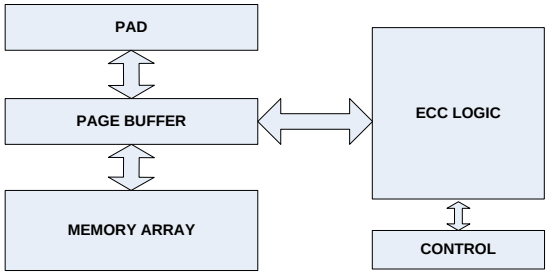
1 Error Correcting Code (ECC)

The NAND flash architecture inherently requires ECC because data can potentially get random bit errors. Depending on the technology node and whether it is single-level cell or multi-level cell (MLC), the number of ECC bits required for correction is different.

SkyHigh 4X-nm SLC NAND flash products recommends having1-bit ECC correction per a 528-byte sector. The 32-nm SLCNAND products require 4-bit ECC correction per a 528-byte sector for the 1-Gb density or 4-bit ECC correction per544-byte sector for all other densities. Some of the newer chipsets or controllers available have the capability ofcorrecting more bits than the NAND requires. This improves data retention provided the NAND has enough sparearea to support parity bit calculation for a higher number of ECC corrections.

The SkyHigh 1X-nm S34ML04G3 SLC NAND Flash memory is designed with a powerful internal ECC engine. The on-die ECC is designed to make S34ML04G3 backward compatible with existing nodes and will work with application processors that have only a 1-bit ECC engine.

2 SkyHigh 1X-nm SLC On-chip ECC Architecture



3 Read Status Register Field Definition

S34ML04G3 offers advanced feature to enhance the reliability of the device and gives the user the tools to monitor the internal ECC correction activities. Bit[4] of the status register coding shown in Table 1 is designed to report ECC correction status. There are two Flag settings available to the user, Flag1 and Flag2, with Flag1 being the default setting. The setting can be changed using the SET_FEATURE command in the Feature Address 90h - Array Operation Mode (P1 register) as shown in table 2. Bit [4] is cleared if internal ECC is off.

- Flag 1 mode (default): When set to 1, bit[4] indicates that the page read had a high ECC error count. When such a situation occurs, the user is recommended to re-program the page read. If cleared to zero, it is in normal state: internal ECC enabled and error counts are in safe level.
- Flag 2 mode: When set to 1, bit[4] indicates that the page read is uncorrectable because it had more ECC errors than the internal ECC engine could correct. If cleared to zero, then it is in normal state: internal ECC enabled and safely working.

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It must be noted that setting Flag 2 mode may prevent the user from getting a warning ahead of any uncorrectable error.

Table 1. Read Status Register Coding

SR Bit	Value Definition	Block Erase	Page Program	Page Read	OTP Block Protect
0 (1)	Pass: "0" Fail: "1"	Pass / Fail	Pass / Fail	Not Used	Pass/Fail
1	Reserved	Not Used	Not Used	Not Used	Not Used
2	Reserved	Not Used	Not Used	Not Used	Not Used
3 (2)	OTP Not Protected: "0" OTP Protected: "1"	Not Used	Not Used	Not Used	Not Protected/ Protected
4 (3)	1: (Flag 1*) Page Recommended to Rewrite 1: (Flag 2) Page Uncorrectable 0: Normal mode or On-die ECC disabled: "0"	Not Used	Not Used	Flag 1 (default) or Flag 2	Not Used
5 (4)	Busy: "0" Ready: "1"	Not Used	Program in progress/ Completed	Not Used	Not Used
6	Busy: "0" Ready: "1"	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy
7 (5)	Protected: "0" Not Protected: "1"	Write Protect	Write Protect	Write Protect	Write Protect

4 Feature Address 90h-Array Operation Mode

READ and PROGRAM operations with internal ECC for the S34ML04G3 can be enabled or disabled by using the SET FEATURE command.

ECC is enabled/disabled as shown by the command sequence in the Feature Address 90h - Array Operation Mode shown in Table 2.

First, the SET FEATURES Register Write (EFh) command is issued, followed by the Array Operation Mode Feature Address (90h). Then, the P1 parameter ECC_EN(Bit 3) is set to enable or disable ECC.

Flag1/Flag2 can be selected by the same command sequence in the Feature Address 90h - Array Operation Mode table. First, the SET FEATURES Register Write (EFh) command is issued, followed by the Array Operation Mode Feature Address (90h). Then, the P1 parameter is set to select Flag1 or Flag2.

Table 2. Feature Address 90h-Array Operation Mode (P1 Parameter)

Bits	Field Name	Function	Default Value	Description
7	Reserved		0	
6	Reserved		0	
5	Reserved		0	
4	ECC_STATUS_SEL	ECC Status register Flag Select	0	0: Flag1 (Default) 1: Flag2 This bit selects the ECC status register Flag. If ECC_EN=0, this bit is a don't care as SR[4] is always set to 0.
3	ECC_EN	ECC enable	1	0: Internal ECC is disabled 1: Internal ECC is enabled (Default)
2	Reserved		0	
1	OTP_LOCK_EN	OTP Protection Enable	0	1: Set OTP Protection (Lock). 0: Power on value The OTP protection is irreversible and becomes effective only if OTP mode is enabled.
0	OTP_MODE_EN	OTP Mode Enable	0	0: Normal (Array operation) 1: OTP mode enable

5 ECC Status with Get Feature

During a READ operation, the page data is read from the array to the data register, where the ECC code is calculated and compared with the value read from the array. If a 1- to 6-bit error per 32 byte is detected, the error is corrected in the cache register. If greater than 6 bit errors are detected, the page is uncorrectable.

The number of error correction per a 32-byte chunk of data can be obtained by using the command sequence in the GET FEATURES command. The number of errors is readable only after a read operation with ECC on.

First, the GET FEATURES (EEh) command is issued, followed by the Array Operation Mode Feature Address shown in Table 3 and Table 4.

NOP0-NOP3 refers to a partial page of 512 bytes for the 2-KB-page device and 1024 bytes for the 4-KB- page device. Each partial page consists of 16 chunks of 32 bytes of data.

For example, in the case of 2-KB-page devices, selecting feature address 0x40 will return 4 bytes of parameters representing the number of errors in each chunk according to Table 3. The number of errors will be displayed using the three least significant bits of the byte (IO2 – IO0) for even blocks and (IO6 – IO4) for odd blocks.

Feature Address 0x50h will return 4 bytes of parameters representing the number of errors in the spare areas of the page.

For the 4-KB-page device, chunks X-0 number or errors will be displayed using (IO2– IO0) while chunks X-1 number of errors will be displayed using (IO6 – IO4).

Table 3. ECC Status – 2-KB-Page Device Option

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
	Reserved	Errors			Reserved	Errors		
Address	**NOP**	**First Byte (P1)**		**Second Byte (P2)**		**Third Byte (P3)**		**Fourth Byte (P4)**
40h	**NOP0**	Chunk 0		Chunk 1		Chunk 2		Chunk 3
41h		Chunk 4		Chunk 5		Chunk 6		Chunk 7
42h		Chunk 8		Chunk 9		Chunk 10		Chunk 11
43h		Chunk 12		Chunk 13		Chunk 14		Chunk 15
44h	**NOP1**	Chunk 0		Chunk 1		Chunk 2		Chunk 3
45h		Chunk 4		Chunk 5		Chunk 6		Chunk 7
46h		Chunk 8		Chunk 9		Chunk 10		Chunk 11
47h		Chunk 12		Chunk 13		Chunk 14		Chunk 15
48h	**NOP2**	Chunk 0		Chunk 1		Chunk 2		Chunk 3
49h		Chunk 4		Chunk 5		Chunk 6		Chunk 7
4Ah		Chunk 8		Chunk 9		Chunk 10		Chunk 11
4Bh		Chunk 12		Chunk 13		Chunk 14		Chunk 15
4Ch	**NOP3**	Chunk 0		Chunk 1		Chunk 2		Chunk 3
4Dh		Chunk 4		Chunk 5		Chunk 6		Chunk 7
4Eh		Chunk 8		Chunk 9		Chunk 10		Chunk 11
4Fh		Chunk 12		Chunk 13		Chunk 14		Chunk 15
50h	**User Spare**	Chunk 0		Chunk 1		Chunk 2		Chunk 3

Table 4. ECC Status- 4-KB-Page Device Option

Address	NOP	First Byte (P1)		Second Byte (P2)		Third Byte (P3)		Fourth Byte (P4)	
40h	NOP0	Chunk0_0	Chunk0-1	Chunk1_0	Chunk1_1	Chunk2_0	Chunk2_1	Chunk3_0	Chunk3_1
41h		Chunk4_0	Chunk4_1	Chunk5_0	Chunk5_1	Chunk6_0	Chunk6_1	Chunk7_0	Chunk7_1
42h		Chunk8_0	Chunk8-1	Chunk9_0	Chunk9_1	Chunk10_0	Chunk10_1	Chunk11_0	Chunk11_1
43h		Chunk12_0	Chunk12_1	Chunk13_0	Chunk13_1	Chunk14_0	Chunk14_1	Chunk15_0	Chunk15_1
44h	NOP1	Chunk0_0	Chunk0-1	Chunk1_0	Chunk1_1	Chunk2_0	Chunk2_1	Chunk3_0	Chunk3_1
45h		Chunk4_0	Chunk4_1	Chunk5_0	Chunk5_1	Chunk6_0	Chunk6_1	Chunk7_0	Chunk7_1
46h		Chunk8_0	Chunk8-1	Chunk9_0	Chunk9_1	Chunk10_0	Chunk10_1	Chunk11_0	Chunk11_1
47h		Chunk12_0	Chunk12_1	Chunk13_0	Chunk13_1	Chunk14_0	Chunk14_1	Chunk15_0	Chunk15_1
48h	NOP2	Chunk0_0	Chunk0-1	Chunk1_0	Chunk1_1	Chunk2_0	Chunk2_1	Chunk3_0	Chunk3_1
49h		Chunk4_0	Chunk4_1	Chunk5_0	Chunk5_1	Chunk6_0	Chunk6_1	Chunk7_0	Chunk7_1
4Ah		Chunk8_0	Chunk8-1	Chunk9_0	Chunk9_1	Chunk10_0	Chunk10_1	Chunk11_0	Chunk11_1
4Bh		Chunk12_0	Chunk12_1	Chunk13_0	Chunk13_1	Chunk14_0	Chunk14_1	Chunk15_0	Chunk15_1
4Ch	NOP3	Chunk0_0	Chunk0-1	Chunk1_0	Chunk1_1	Chunk2_0	Chunk2_1	Chunk3_0	Chunk3_1
4Dh		Chunk4_0	Chunk4_1	Chunk5_0	Chunk5_1	Chunk6_0	Chunk6_1	Chunk7_0	Chunk7_1
4Eh		Chunk8_0	Chunk8-1	Chunk9_0	Chunk9_1	Chunk10_0	Chunk10_1	Chunk11_0	Chunk11_1
4Fh		Chunk12_0	Chunk12_1	Chunk13_0	Chunk13_1	Chunk14_0	Chunk14_1	Chunk15_0	Chunk15_1
50h	User Spare	Chunk0_0	Chunk0-1	Chunk1_0	Chunk1_1	Chunk2_0	Chunk2_1	Chunk3_0	Chunk3_1

I/O2 - I/O0 I/O6 - I/O4	ECC Status
000	No Error
001	1 bit error
010	2 bit error
011	3 bit error
100	4 bit error
101	5 bit error
110	6 bit error
111	Uncorrectable Error

6 Why 1-bit External ECC Correction Is Recommended

S34ML04G3 recommends a 1 bit per 528 bytes external ECC correction capability. With the internal ECC function, the memory delivers corrected data to the page buffer. However, not having any external ECC correction capabilities leave the buffer, the system bus, and the host buffer vulnerable to storage and transmission errors. Therefore, it recommended that the host provide at least 1 bit per 528 bytes ECC correction capability for such protection.

The function of the recommended1-bit external ECC is not to protect the bits during storage in NAND cells; it is only for protecting the data buffers and bus from any additionally induced errors during data transmission.

7 References

- S34ML04G3 4 Gb, 3 V, 2K Page Size, x8 I/O SLC NAND Flash Memory for Embedded, Datasheet, Specification Number 002-19204
- S34ML04G3 4 Gb, 3 V, 4K Page Size, x8 I/O SLC NAND Flash Memory for Embedded, Datasheet, Specification Number 002-19822

Document History

Document Title: AN223237 - S34ML04G3 Internal ECC Corrections and Status

Document Number: 002-23237

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	6097907	MNAD	03/15/2018	New Application Note
*A		MNAD	05/02/2019	Updated to SkyHigh format
*B		MNAD	05/21/2019	Changed the 1 bit ECC from required to recommended

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