Migration from SkyHigh S34ML-1 to S34ML-3 4K Page SLC NAND

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Associated Part Families: **S34ML-1, S34ML-3**

AN222053 details how to migrate existing designs from SkyHigh S34ML-1 NAND flash memory (S34ML04G1) to SkyHigh S34ML-3 NAND flash memory (S34ML04G3-2k page).

1 Introduction

This application note summarizes the differences between SkyHigh S34ML-1 and S34ML-3 NAND flash memory families and details how to migrate designs from S34ML-1 to S34ML-3. S34ML-1 devices are 3.3 V NAND flash memoryparts manufactured with 48-/41-nm technology. S34ML-3 devices are 3.3 V NAND flash memory parts manufactured with 16-nm technology.

Note: The information provided in this application note focuses on the differences between the two device families. See the respective datasheets for more information and full specifications.

2 Feature Overview

Most features are identical in both device families. For example, SkyHigh S34ML04G3 NAND flash devices are compatible with the S34ML04G1 NAND flash family; both have the following similar characteristics:

- Unique ID (serial number)
- One-Time-Programmable (OTP) area
- 10 Years data retention
- ONFI 1.0 compliance
- JEDEC standard-compliant software command set

Table 1 lists the important differences.

Table 1. Feature Differences

Features	S34ML04G1	S34ML04G3
Page size	2 KB	4 KB
Spare area per page	64 bytes	128 bytes
Number of planes	2	1
User level ECC correction	1-bit	0-bit
Cache read/write	✓	–
Volatile block protection	–	✓
Permanent block protection	–	✓
Unique ID	–	✓
Page read (t_R)	25 µs max	55 µs typ
Read cycle time (t_{RC} min)	25 ns (ONFI mode 4)	20 ns (ONFI mode 5)
Program time (t_{PROG} typ)	200 µs	400 µs
Block erase time (t_{BERS} typ)	2 ms (1 Gb), 3.5 ms (2/4 Gb)	4.0 ms

Reliability	100,000 P/E cycles	60,000 P/E cycles
OTP block	0	3
Packages	TSOP-48, BGA-63	TSOP-48, BGA-63, BGA-67

3 Device Identification and Configuration

Table 2 lists the differences in ONFI Parameter Page between S34ML04G1 and S34ML04G3. Software that uses dynamic adaptive ONFI probing should work without changes.

Table 2. ONFI Parameter Page Differences

Byte	Description	S34ML04G1	S34ML04G3
6-7	Features supported [4] Odd-to-even page copyback [3] Interleaved operations [2] Non-sequential page program [1] Multiple LUN operations [0] 16-bit data bus width	1Ch, 00h	10h, 00h
8-9	Optional commands supported [5] Read Unique ID [4] Copyback [3] Read Status Enhanced [2] Get/Set Features [1] Read Cache [0] Page Cache Program	1Bh, 00h	3Ch, 00h
44-63	Device model	S34ML04G1: 53h, 33h, 34h, 4Dh, 4Ch, 30h, 34h, 47h, 31h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h	S34ML04G3: 53h, 33h, 34h, 4Dh, 4Ch, 30h, 34h, 47h, 33h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
80-83	Number of data bytes per page	00h, 08h, 00h, 00h	00h, 10h, 00h, 00h
84-85	Number of spare bytes / page	40h, 00h	00h, 01h
86-89	Number of data bytes per partial page	00h, 02h, 00h, 00h	00h, 04h, 00h, 00h
90-91	Number of spare bytes / partial page	10h, 00h	40h, 00h
96-99	Number of blocks per logical unit (LUN)	00h, 10h, 00h, 00h	00h, 08h,00h,00h
103-104	Bad blocks maximum per LUN	50h, 00h	28h, 00h
105-106	Block endurance	01h, 05h	06h, 04h
107	Guaranteed valid blocks at beginning	01h	08h
108-109	Endurance for guaranteed valid blocks	01h, 03h	00h, 00h
112	Number of bits ECC correctability	01h	00h
113	Number of interleaved address bits	01h	01h
114	Interleaved operation attributes [3] restrictions for program cache [2] program cache supported [1] no block address restrictions [0] interleaving support	04h	00h
129-130	Timing mode support [5] timing mode 5 [4] timing mode 4 [3] timing mode 3 [2] timing mode 2 [1] timing mode 1 [0] timing mode 0	1Fh, 00h	3Fh, 00h

Byte	Description	S34ML04G1	S34ML04G3
131-132	Program Cache timing mode support [5] timing mode 5 [4] timing mode 4 [3] timing mode 3 [2] timing mode 2 [1] timing mode 1 [0] timing mode 0	1Fh, 00h	00h, 00h
133-134	Maximum page program time (µs)	BCh, 02h	58h, 02h
137-138	Maximum page read time (µs)	19h, 00h	5Eh, 01h
139-140	Minimum Change Column setup time (ns)	64h, 00h	C8h, 00h
254-255	Integrity CRC	45h, 8Eh	21h, E8h

Table 3 lists the device IDs for the S34ML-1 and S34ML-3 device family members. If the software uses a hardcoded device ID parameter table, new entries for S34ML-3 must be added.

Table 3. Device IDs

Command	S34ML04G1	S34ML04G3
Read ID	01h, DCh, 90h, 95h, 54h (4 Gb)	01h, DCh, 00h, 1Ah, 00h (4 Gb)

4 AC Characteristics

S34ML-1 and S34ML-3 families have mainly AC-compatible specifications. Table 4 lists the differences in AC characteristics between the devices. Apart from the page read time (data transfer time from cell to register), the S34ML-3 family is faster in every aspect when compared to the S34ML-1 family. This means that the existing S34ML-1 timings should work fine for S34ML-3 parts.

Table 4. AC Characteristics Differences

Parameter	S34ML-1	S34ML-3
CE# setup time (t_{CS} min)	20 ns	15 ns
Data setup time (t_{DS} min)	10 ns	7 ns
Page read (t_{R})	25 µs max	55 µs typ
Read cycle time (t_{RC} min)	25 ns	20 ns
RE# access time (t_{REA} max)	20 ns	16 ns
RE# high hold time (t_{REH} min)	10 ns	7 ns
RE# pulse width (t_{RP} min)	12 ns	10 ns
Write cycle time (r_{WC} min)	25 ns	20 ns
WE# high hold time (t_{WH} min)	10 ns	7 ns
WE# pulse width (t_{WP} min)	12 ns	10 ns

This also applies to power-on timing requirements. S34ML-1 devices initialize within 5 ms, whereas S34ML04G3 parts require just 3 ms to initialize (after the reset command). For S34ML04G3 parts, it is required to send a reset command (FFh) after power-on and it is recommended to keep WP# LOW during power up and down.

5 DC Characteristics

S34ML04G1 and S34ML-3 families have mainly DC-compatible specifications. Table 5 lists the differences in DC characteristics between the devices. During power ON and in standby mode, the S34ML04G3 family requires slightly higher current than the S34ML-1 family. The potential impact of these differences should be evaluated and validated.

Table 5. DC Characteristics Differences

Parameter	S34ML-1	S34ML-3
Power on current (I_{CC0} max)	30 mA	50 mA
Sequential read current (I_{CC1} max)	30 mA	35 mA
Program current (I_{CC2} max)	30 mA	35 mA
Standby current, CMOS (I_{CC5} max)	50 µA	100 µA

6 Packages

S34ML04G3 parts are available in the same TSOP-48 and BGA-63 packages as S34ML04G1. In addition, a new BGA-67 package is offered for S34ML04G3.

The S34ML04G3 family adds a new Volatile Protection Enable (VPE) signal that is connected to TSOP-48 pin #38 and BGA-64 ball G5, respectively. Both are NC for the S34ML04G1 family and have a weak internal pull-down in S34ML-3 parts to disable the VPE feature if the input is left floating. This guarantees compatibility with existing board layouts.

7 References

Datasheets:

- 002-00676 - S34ML01G1, S34ML02G1, S34ML04G1 1 GBIT, 2 GBIT, 4 GBIT, 3 V SLC NAND FLASH FOR EMBEDDED
- 002-19822 - S34ML04G3, 4 GB, 3 V, 4K PAGE SIZE, x8 I/O, SLC NAND FLASH MEMORY FOR EMBEDDED (ADVANCE)

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5968846	MNAD	11/17/2017	
*A		MNAD	05/22/2019	Updated to SkyHigh format Changed 1-bit ECC to 0-bit ECC for S34ML-3 in the Features and Parameter Page sec.