Migration from SkyHigh S34ML-1 to S34ML-3-2K Page SLC NAND

Author: Gernot Hoyler

Associated Part Families: S34ML-1, S34ML-3

Related Application Notes: AN200516

AN219369 details how to migrate existing designs from SkyHigh S34ML-1 NAND flash memory (S34ML04G1) to SkyHigh S34ML-3 NAND flash memory (S34ML04G3-2K page).

1 Introduction

This application note summarizes the differences between the SkyHigh S34ML04G1 and S34ML04G3 NAND flash
memory devices. It details how to migrate designs from S34ML04G1 to S34ML04G3. S34ML04G1 devices are 3.3-V NAND flash memory parts manufactured with 48-nm or 41-nm technology. S34ML04G3 devices are 3.3-V NAND flash memory parts manufactured with 16-nm technology.

Note: The information provided in this application note focuses on the differences between the two device families. Refer to the respective datasheets for further information and full specifications.

2 Feature Overview

Many features of the two device families are identical. For example, SkyHigh S34ML04G3 NAND flash devices are compatible with the S34ML04G1 NAND flash; both have the following similar characteristics:

- 2048 data bytes per page, 64 pages per block,
- ONFI 1.0 compliance
- JEDEC standard-compliant software command set

Table 1 summarizes the most important differences.

Table 1. Feature Differences

Features	S34ML04G1	S34ML04G3
Spare area per page	64 bytes	128 bytes
User level ECC correction	1-bit	0-bit
Cache read/write	✓	–
Volatile block protection	–	✓
Permanent block protection	–	✓
Unique ID	–	✓
Page read (t_R)	25 µs max	45 µs typ on single plane
Read cycle time (t_{RC} min)	25 ns (ONFI mode 4)	20 ns (ONFI mode 5)
Program time (t_{PROG} typ)	200 µs	350 µs
Block erase time (t_{BERS} typ)	3.5 ms	4.0 ms
Reliability	100,000 P/E cycles	60,000 P/E cycles
OTP Block number	0	6

Features	S34ML04G1	S34ML04G3
Packages	TSOP-48, BGA-63	TSOP-48, BGA-63, BGA-67

3 Device Identification and Configuration

Table 2 shows the differences in the ONFI parameter page between S34ML04G1 and S34ML04G3. Software that uses dynamic adaptive ONFI probing should work without changes.

Table 2. ONFI Parameter Page Differences

Byte	Description	S34ML04G1	S34ML04G3
6-7	Features supported [4] odd-to-even page copyback [3] interleaved operations [2] non-sequential page program [1] multiple LUN operations [0] 16-bit data bus width	1Ch, 00h	18h, 00h
8-9	Optional commands supported [5] Read Unique ID [4] Copyback [3] Read Status Enhanced [2] Get/Set Features [1] Read Cache [0] Page Cache Program	1Bh, 00h	3Ch, 00h
44-63	Device model	S34ML04G1: 53h, 33h, 34h, 4Dh, 4Ch, 30h, 34h, 47h, 31h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h	S34ML04G3: 53h, 33h, 34h, 4Dh, 4Ch, 30h, 34h, 47h, 33h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
84-85	Number of spare bytes/page	40h, 00h	80h, 00h
90-91	Number of spare bytes/partial page	10h, 00h	20h, 00h
105-106	Block endurance	01h, 05h	06h, 04h
107	Guaranteed valid blocks at beginning	01h	08h
108-109	Endurance for guaranteed valid blocks	01h, 03h	00h, 00h
112	Number of bits ECC correctability	01h	00h
114	Interleaved operation attributes [3] restrictions for program cache [2] program cache supported [1] no block address restrictions [0] interleaving support	04h	00h
129-130	Timing mode support [5] timing mode 5 [4] timing mode 4 [3] timing mode 3 [2] timing mode 2 [1] timing mode 1 [0] timing mode 0	1Fh, 00h	3Fh, 00h
131-132	Program cache timing mode support [5] timing mode 5	1Fh, 00h	00h, 00h

Byte	Description	S34ML04G1	S34ML04G3
	[4] timing mode 4 [3] timing mode 3 [2] timing mode 2 [1] timing mode 1 [0] timing mode 0		
133-134	Maximum page program time (µs)	BCh, 02h	58h, 02h
137-138	Maximum page read time (µs)	19h, 00h	C2h, 01h
139-140	Minimum change column setup time (ns)	64h, 00h	C8h, 00h
254-255	Integrity CRC	45h, 8Eh	F1h, 2Bh

Table 3 shows the device IDs for S34ML04G1 and S34ML04G3. If software uses a hardcoded device ID parameter table, new entries for S34ML04G3 must be added.

Table 3. Device IDs

Command	S34ML04G1	S34ML04G3
Read ID	01h, DCh, 90h, 95h, 54h (4 Gb)	01h, DCh, 00h, 05h, 04h (4 Gb)

4 AC Characteristics

The S34ML04G1 and S34ML04G3 devices have mainly compatible AC specifications. Differences in AC characteristics between the devices are highlighted in Table 4. Apart from the page read time (data transfer time from cell to register), the S34ML-3 family is faster in every respect compared to the S34ML04G1 device. This means that existing S34ML04G1 timings should work for S34ML04G3 parts.

Table 4. AC Characteristics Differences

Parameter	S34ML-1	S34ML-3
CE# setup time (t_{CS} min)	20 ns	15 ns
Data setup time (t_{DS} min)	10 ns	7 ns
Page read (t_R)	25 µs max	55 µs typ single plane (90 µs multi plane)
Read cycle time (t_{RC} min)	25 ns	20 ns
RE# access time (t_{REA} max)	20 ns	16 ns
RE# high hold time (t_{REH} min)	10 ns	7 ns
RE# pulse width (t_{RP} min)	12 ns	10 ns
Write cycle time (r_{WC} min)	25 ns	20 ns
WE# high hold time (t_{WH} min)	10 ns	7 ns
WE# pulse width (t_{WP} min)	12 ns	10 ns

This also applies to power-on timing requirements. S34ML04G1 devices initialize within 5 ms, whereas S34ML04G3 parts require only 3 ms to initialize (after the reset command). For S34ML04G3 parts, a reset command (FFh) should be sent after power-on and it is recommended to keep WP# LOW during power up and down.

5 DC Characteristics

S34ML04G1 and S34ML04G3 have mainly compatible DC specifications. Differences in DC characteristics between the devices are highlighted in Table 5. During power on and in standby mode, the S34ML04G3 requires higher current than the S34ML04G1 device. The potential impact of these differences should be evaluated and validated.

Table 5. DC Characteristics Differences

Parameter	S34ML-1	S34ML-3
Power on current (I_{CC0} max)	30 mA	50 mA
Sequential read current (I_{CC1} max)	30 mA	35 mA
Program current (I_{CC2} max)	30 mA	35 mA
Standby current, CMOS (I_{CC5} max)	50 µA	100 µA

6 Packages

S34ML04G3 parts are available in the same TSOP-48 and BGA-63 packages as S34ML04G1. In addition, a new BGA-67 package is offered for S34ML04G3.

The S34ML04G3 device adds a new volatile protection enable (VPE) signal that is connected to TSOP-48 pin #38 and BGA-64 ball G5, respectively. Both are NC for the S34ML04G1 device and have a weak internal pull-down in S34ML-3 parts to disable the VPE feature if the input is left floating. This guarantees compatibility with existing board layouts.

7 References

- 1 Gb, 2 Gb, 4 Gb, 3 V SLC NAND Flash Memory for Embedded, Datasheet, Specification Number 002-00676.
- 4 Gb, 3 V SLC NAND Flash Memory for Embedded, Datasheet, Specification Number 002-19204

Document History

Document Title: AN219369 - Migration from SkyHigh S34ML-1 to S34ML-3-2K Page SLC NAND

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5726250	GEHO	04/12/2017	New application note
*A	5971498	MNAD	11/20/2017	Removed 1 Gb and 2 Gb devices Updated performance number and parameter page values
*B		MNAD	05/22/2019	Updated to SkyHigh format Changed 1-bit ECC to 0-bit ECC for S34ML-3 in Features and Parameter Page sec.