Single Flash Image for Multiple SLC NAND Flash Devices With Different Sizes of Spare or OOB Area

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AN218226 shows how to create a product that uses a single flash image with SLC NAND flash from multiple suppliers, where a SkyHigh flash part with 64B or 128B spare area is used with another compatible NAND flash device with a different spare area size. Required changes are shown for the general case. Modifications to the LinuxMTD are provided to illustrate one of the required changes for Linux-based systems.

1 Introduction

This application note assumes that the reader is familiar with creating, programming, and validating NAND flash images for products that are built using a single source for the NAND memory chip.

If your design uses NAND flash devices from other vendors along with a SkyHigh SLC NAND chip with 2 KB main area, 64B or larger spare area, and automatic Open NAND Flash Interface (ONFI) parameter page scans, thefollowing issues may arise:

1. Various software components automatically choose a page size that may not match the page size that was used to create the single flash image.
2. ECC correction power automatically chosen by an ONFI parameter page scan does not match the ECC correction power that was used to create the single flash image.
3. Software may self-configure to a different page format that is encoded into the single flash image. This may cause problems if a second device with a different page size and/or a different ECC correction power requirement is brought online after the primary NAND source is qualified and in production with the original flash image.

This application note highlights the areas where different page sizes or ECC correction power requirements can cause problems so that you can plan for a smooth introduction of the second source. If all NAND flash chips in your sourcing plan have identically sized spare areas and have identical requirements for ECC correction power, your existing flash image will not encounter the issues described in this document.

SkyHigh SLC NAND devices have 64 pages per block per plane where the pages have a 2-KB main area and a spare area size of either 64B or 128B. Table 1 lists the spare area sizes and minimum required ECC correction power for two generations of SkyHigh SLC NAND products. In addition, note the following:

1. Densities greater than 1 Gb from the S34ML-2 and S34MS-2 product families have a 128B spare area while the rest of the listed devices have a 64B spare area.
2. ECC correction power requirement varies per partial page (528B):
    a. S34Mx-1: At least one bit of ECC correction power
    b. S34Mx-2: At least four bits of ECC correction power

The considerations noted in this application note apply to these SkyHigh SLC NAND product families when they are used alongside other flash chips with differing spare area sizes and/or differing minimum ECC correction powerrequirements.

Table 1. Spare Area Size and ECC Requirement for SkyHigh SLC NAND Flash

Family	Spare Area Size (B)	Minimum Bits of ECC Protection
S34ML01G1 S34MS01G1 S34ML02G1 S34MS02G1 S34ML04G1 S34MS04G1 S34ML08G1	64	1
S34ML01G2 S34MS01G2	64	4
S34ML02G2 S34MS02G2 S34ML04G2 S34MS04G2 S34ML08G2 S34MS08G2 S34ML16G2 S34MS16G2	128	4

2 NAND Flash Image Format

Table 2 shows some examples of NAND flash products that have 2-KB main area sizes, and various spare area sizes and ECC requirements.

Table 2. Spare Area Size and ECC Requirement for a Sample of Available 2-KB Page SLC NAND Flash

Product Line	Spare Area Size (B)	Minimum Bits of ECC Protection
SkyHigh S34ML-1	64	1
SkyHigh S34ML-2	64 or 128	4
Macronix MX30LF-28AB	112	8
Micron M29F2G	224	8

Question: What page size and ECC correction power should you use for your flash image format?

Answer: Check the datasheets for the flash devices in your sourcing plan and identify the device having the smallest spare area size, and the device requiring the highest number of bits of ECC correction power. The smallest page size and the highest ECC correction power must be hard-coded into all software modules that access your single flash image. Your programming tools may also require similar consideration.

Question: My sourcing plan is using the SkyHigh S34ML02G2 and the Macronix MX30LF2G28AB. How should I configure my page format?

Answer: Use a spare area size of 112B and ECC that provides 8 bits of correction per partial page.

Question: My sourcing plan is using the SkyHigh S34ML02G2 and the Micron M29F2GxxAxAF. How should I configure my page format?

Answer: Use a spare area size of 128B and ECC that provides 8 bits of correction per partial page.

Question: My sourcing plan is using the SkyHigh S34ML01G2 and the SkyHigh S34ML02G2. How should I configure my page format?

Answer: Use a spare area size of 64B and ECC that provides 4 bits of correction per partial page.

3 Automatic ONFI Parameter Page Scan

If any of your code modules scan the ONFI parameter page, ensure that you do not use this scan to set your NAND page size or ECC correction power.

Here is a list of items to check to make sure that all automatic ONFI parameter page scans have been replaced with a single, hard-coded page size and ECC correction power:

- primary boot loader
- secondary boot loader
- application code
- data storage code

The data storage code has two subcases:

- If production programming leaves the data partition blank (i.e., erased and unformatted), then the data storage code may scan the ONFI parameter page to configure the flash page size before formatting the data partition upon first boot. File downloads may be done over the wire or over the air in subsequent production steps or after the product is deployed.
- If production programming uses a flash image with a pre-formatted data partition, i.e., a formatted partition that is either empty or that contains files, then the flash page size must be hard-coded in the data storage software.

4 Linux Automatic ONFI Parameter Page Scan

Linux scans the ONFI parameter page in the MTD code to automatically choose the flash page size. The ECC correction power is automatically maximized based on the identified Out Of Band (OOB) or spare area size.

If the MTD is used for boot loaders and data storage, there may be multiple independent copies of the MTD in your system – each copy needs to be changed. SkyHigh provides a patch, reproduced here, that hard-codes the page size used by the MTD to 2 KB + 128B. You may need to adjust this page size to match your sourcing plan.

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---------------------------------------------------------------------------------------------------------
This program is free software; you can redistribute it and/or modify it under the terms of
the GNU General Public License version 2 as published by the Free Software Foundation.
---------------------------------------------------------------------------------------------------------
diff -rupN linux-3.14.27-100.fc19.i686/drivers/mtd/nand/nand_base.c linux-3.14.27-
65nm/drivers/mtd/nand/nand_base.c
--- linux-3.14.27-100.fc19.i686/drivers/mtd/nand/nand_base.c 2014-03-31 05:40:15.000000000
+0200
+++ linux-3.14.27-65nm/drivers/mtd/nand/nand_base.c 2016-04-19 10:58:38.761683716 +0200
@@ -3129,6 +3129,12 @@ static int nand_flash_detect_onfi(struct
mtd->erasesize *= mtd->writesize;
mtd->oobsize = le16_to_cpu(p->spare_bytes_per_page);
+ if ((strcmp(p->model,"S34ML02G2") == 0 ||
+ strcmp(p->model,"S34ML04G2") == 0 ||
+ strcmp(p->model,"S34ML08G2") == 0 ||
+ strcmp(p->model,"S34ML16G2") == 0 ||
+ strcmp(p->model,"S34MS02G2") == 0 ||
+ strcmp(p->model,"S34MS04G2") == 0 ||
+ strcmp(p->model,"S34MS08G2") == 0 ||
+ strcmp(p->model,"S34MS16G2") == 0 ) && mtd->oobsize == 128) {
+ printk("Setting OOB size to 64\n");
+ mtd->oobsize = 64;
+ }
/* See erasesize comment */
chip->chipsize = 1 << (fls(le32_to_cpu(p->blocks_per_lun)) - 1);
        ---------------------------------------------------------------------------------------------
```

5 Production Programming

Production programmers may use ONFI parameter page scans to learn the physical page size in the flash. The programmer then completely fills the pages from the binary image file you supply. If the page size assumed by your flash image does not match the physical page size, page breaks in the programmed image will be wrong. Check with your programming house to ensure that their programmer inserts the page breaks at the right location for your image. For flash devices with larger than the minimum spare area size from your sourcing plan, this will leave blank space at the end of each page that won't be used by any of your boot loaders, application code, or data storage code that have been modified according to the guidance in this application note.

This mitigation may impact the bad block scheme used by the production programming house. You should verify that any impacts are managed.

ECC correction power, ECC algorithm, and the column location of the ECC bits in the page format are standard items that you specify to configure the programmer – just make sure this matches the choice you made for the page format in your single flash image.

6 Conclusion

Using SkyHigh SLC NAND flash alongside SLC NAND flash chips from other suppliers, where the spare or OOB areas are of different sizes, may cause production issues or functional issues for your product when a new flashsource is introduced to production. Planning for a trouble-free introduction of your alternate NAND source is easilymanaged by using the guidance provided in this application note.

Document History

Document Title: AN218226 - Single Flash Image for Multiple SLC NAND Flash Devices With Different Sizes of Spare or OOB Area

Document Number: 002-18226

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5558330	MNAD	03/01/2017	Initial release
*A		MNAD	05/24/2019	Updated to SkyHigh format