# Programming Multiple SkyHigh NAND Flash Devices for a Single Product

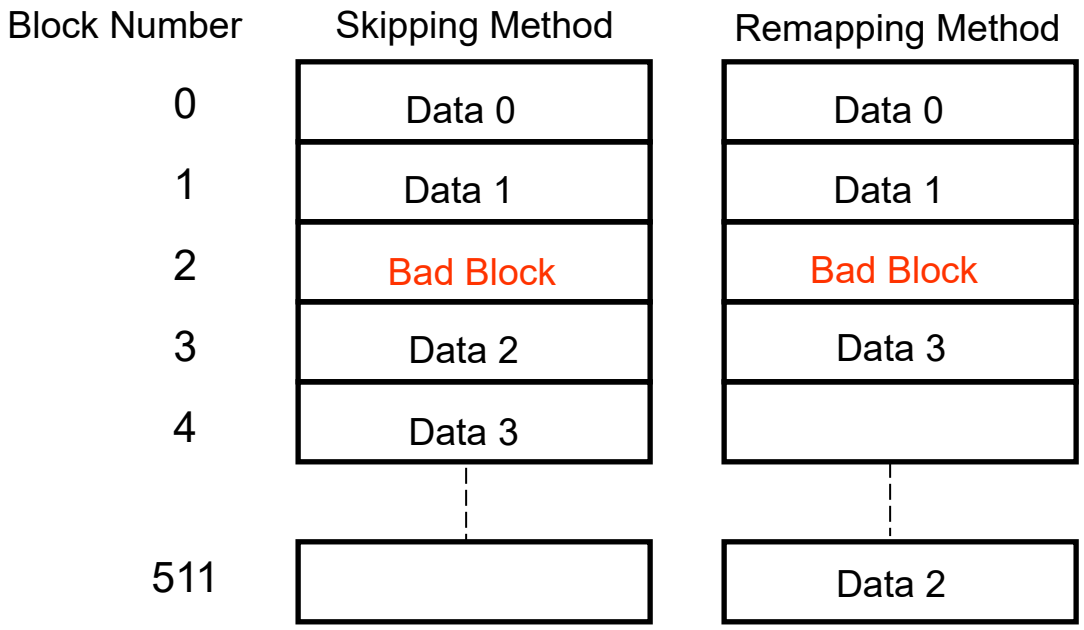
AN203229 describes the steps involved in preparing a master “golden” image that can be used to program multiple NAND devices for the same platform or product.

## 1 Introduction

NAND Flash memory is a natural fit for data storage in a wide range of embedded systems. Due to the limited resources available in these platforms, system designers often choose to store code and firmware in NAND as well. Although booting from NAND Flash is supported by many chipsets, this is more complex than booting from memory devices that are mapped directly into memory address space for XIP (eXecute In Place). Booting a system from NAND Flash generally requires multiple stages of boot-loaders. Each stage of loader firmware and the run-time code that accesses NAND Flash must include the code necessary to interface with the particular NAND controller and any NAND Flash devices that will be supported. Planning support for multiple NAND devices allows OEMs flexibility in case of a supply shortage or cost-savings by selecting a less expensive part.

## 2 NAND Bad Blocks

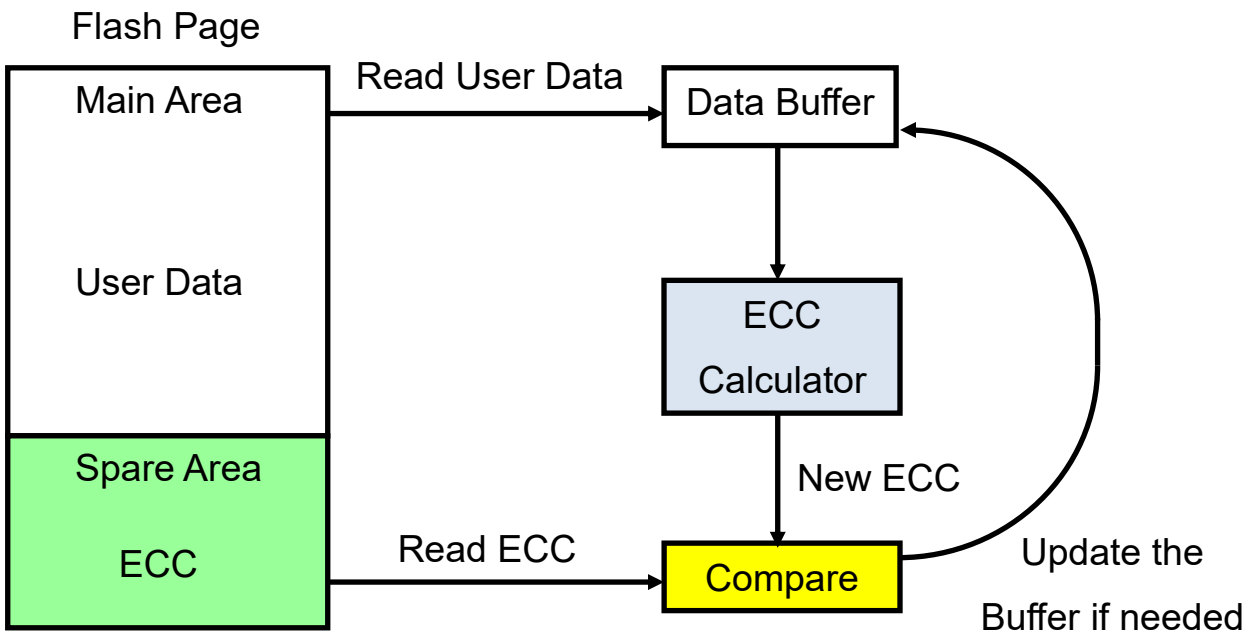
NAND Flash chips can be shipped with initial bad blocks from the factory, and blocks can become bad during usage. These bad blocks are either skipped or remapped into a reserved area.



NAND device programmers must detect initial bad blocks as well as errors reported by the Flash device during erase and program operations. The initial bad block marking and error status are defined in the NAND device data sheet(s). There are differences between some NAND devices in these areas. Programmers must work around any bad blocks detected for each chip and record the bad block information in a way that will be understood by the run-time code and boot-loaders. NAND Flash data sheets generally specify that at least 98% of the blocks will be good within the rated endurance of the device. The image to be programmed must be at least 2% smaller than the total device density to allow for bad blocks.

# 3 NAND Error Correcting Codes (ECC)

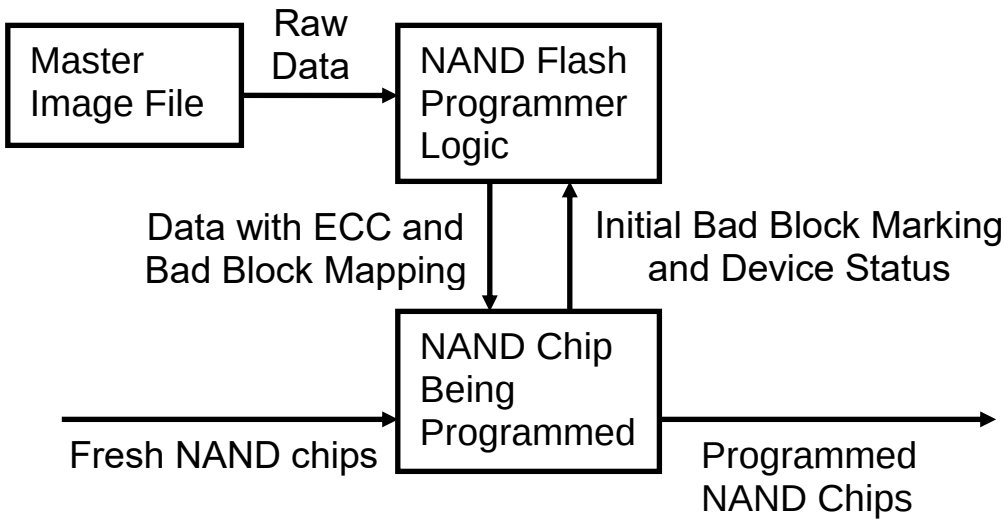
NAND Flash chips are allowed a small number of bit errors, which can be corrected after a read operation with Error Correcting Codes (ECC). ECC syndrome bits are calculated from the data to be programmed and stored along with the data, in the spare area. The spare area is also called the out-of-band (OOB) area. During a read operation, another ECC syndrome is calculated from the data that was read and compared to the ECC syndrome that was stored in the spare area.




NAND device data sheets typically require 1- or 4-bit ECC per 512 bytes of data (528 bytes including metadata). Some NAND controllers include ECC calculation in hardware. If the required ECC is not supported by the NAND controller, it can be implemented in software. Some NAND controllers enforce a particular format for the location of ECC bits within the spare area. Some NAND firmware and software require a particular format for the ECC bits within the spare area. The system designer must ensure that all components use the same ECC algorithms and spare area format, including the NAND Flash programmer. The image to be programmed should not contain the ECC syndrome bits. These should be calculated by the NAND programmer at the time the image is being written to Flash.

# 5 NAND Flash Programming

NAND Flash memory programmers use a master image file to write data to a number of NAND chips. Generally, the image file is created with a specific NAND device in mind. The programmer must write ECC syndrome bits in the spare area for each page, using a format that will be recognized by the target system, and an ECC algorithm that will be both recognized by the target system, and sufficient to meet the NAND device specification. The programmer must recognize bad blocks according to the NAND device specification and map any bad blocks using a method that will be supported by the target system.




NAND Flash memory programmers generally detect the characteristics of the device to be programmed and program the image file, starting at a given offset, and filling each page with data before proceeding to the next page. This approach cannot support NAND devices with different size pages. Also, if the NAND devices to be programmed differ in terms of density, ECC requirements, or bad block markings, these differences must be considered in creating the master image file and in configuring the device programmer.

# 6 SkyHigh NAND Flash Characteristics

SkyHigh NAND devices are available with different physical characteristics. All of these devices support ONFI 1.0 for detection of device characteristics.

| Part Number | Supply Voltage | Device Size | Main Page Size | Spare Area Size* | ECC required |
|---|---|---|---|---|---|
| S34ML08G1 | 3 V | 1 GB | 2 KB | 64 B | 1 bit |
| S34ML04G1 | 3 V | 512 MB | 2 KB | 64 B | 1 bit |
| S34ML02G1 | 3 V | 256 MB | 2 KB | 64 B | 1 bit |
| S34ML01G1 | 3 V | 128 MB | 2 KB | 64 B | 1 bit |
| S34ML16G2 | 3 V | 2 GB | 2 KB | 128 B | 4 bit |
| S34ML08G2 | 3 V | 1 GB | 2 KB | 128 B | 4 bit |
| S34ML04G2 | 3 V | 512 MB | 2 KB | 128 B | 4 bit |
| S34ML02G2 | 3 V | 256 MB | 2 KB | 128 B | 4 bit |
| S34ML01G2 | 3 V | 128 MB | 2 KB | 64 B | 4 bit |
| S34MS04G1 | 1.8 V | 512 MB | 2 KB | 64 B | 1 bit |
| S34MS02G1 | 1.8 V | 256 MB | 2 KB | 64 B | 1 bit |
| S34MS01G1 | 1.8 V | 128 MB | 2 KB | 64 B | 1 bit |
| S34MS16G2 | 1.8 V | 2 GB | 2 KB | 128 B | 4 bit |
| S34MS08G2 | 1.8 V | 1 GB | 2 KB | 128 B | 4 bit |
| S34MS04G2 | 1.8 V | 512 MB | 2 KB | 128 B | 4 bit |
| S34MS02G2 | 1.8 V | 256 MB | 2 KB | 128 B | 4 bit |
| S34MS01G2 | 1.8 V | 128 MB | 2 KB | 64 B | 4 bit |

*Note: The spare area in each page is also called the out-of-band (OOB) area.

# 7 Supporting Multiple NAND Devices

Using the following steps, a master “golden” image can be generated to support multiple different NAND Flash devices.

**Step 1:** Identify the full list of NAND Flash devices to be supported and the characteristics of each. Refer to table 1.1 above.

**Step 2:** Identify the smallest number of columns per page for every NAND Flash device to be supported, where “N” = this number of columns.

**Step 3:** Identify the worst-case ECC requirement for all devices to be supported

**Step 4:** Choose a single page format that satisfies the worst-case ECC requirement and uses the minimum page size (fits within “N” columns).

**Step 5:** Choose a single bad block management method that will meet the specifications for all supported devices and will be used and understood by all run-time code and boot-loaders. Most bad block management schemes use a table written into at least two blocks when the master image is programmed to the NAND device.

**Step 6:** Implement all run-time code, boot-loaders, and preliminary data partitions using this page format (“N” columns). Do not use automatic configuration based on the ONFI Parameter Page, ID codes, or any other detection method.

> **Note:** Automatic configuration can be used on data partitions that are not programmed at production time, but are formatted after the initial system startup.

**Step 7:** The production programmer must use the page size selected above (“N” columns), not the actual page size of the device, which may be larger. This allows the programmer to correctly program the master image file into the first “N” columns of each page.

**Step 8:** The production programmer must use the selected bad block management method.

**Step 9:** Create the golden master image file. This file should consist of a sequence of pages, each with “N” columns.

**Step 10:** Use the golden master image file and the properly configured programmer to program any of the NAND devices selected in Step 1.

# 8 Conclusion

Following these steps requires attention to detail in various aspects of system design and configuring the production line, but this approach provides advantages in the product production phase. These advantages include flexibility in device selection and potential cost savings.

## Document History

Document Title: AN203229 - Programming Multiple SkyHigh NAND Flash Devices for a Single

Product Document Number: 002-03229

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | – | BWHA | 04/22/2015 | Initial Version |
| *A | 4968187 | BWHA | 10/16/2015 | Updated to Cypress template |
| *B | 5812529 | AESATMP9 | 07/12/2017 | Updated logo and copyright. |
| *C | 6295927 | MNAD | 08/30/2018 | Updated template |
| *D | 6311826 | YOQI | 09/17/2018 | Removed S34MS08G1 from Cypress NAND Flash Characteristics |
| *E | | MNAD | 05/24/2019 | Updated to SkyHigh format |