Thermal Considerations and Parameters

AN201006 discusses the thermal considerations and parameters when using SkyHigh devices in printed wiring board (PWB) geometrics.

1 Introduction

As printed wiring board (PWB) geometries become increasingly more complex and available surface area continues to shrink, the thermal considerations in the assembly become more and more important. Although SkyHigh products are typically very low power, the effect of localized heating due to neighboring high-output devices can be significant. This application note was written with the intent to clarify some of these issues that affect the users of SkyHigh products.

2 General

Thermal analysis and the various mathematical, experimental, and numerical techniques used to model and predict the thermal state of a particular system are governed by the JESD51 family of specifications. Specific thermal models (outside the scope of this application note) are governed by the JESD15 family of specifications. Although thermal analyses have been in use for a number of decades, the associated techniques and methodologies are not evolving at the same rate as the number of new packages and technologies is expanding. This results in outdated and sometimes conflicting information. This application note is intended to summarize the key factors and mathematical parameters used in thermal analysis and to explain it in a manner that is both useful and informative. A good deal of the content is obtained from the reference documents in Section 10, *References* on page 6.

3 Measurement Basics

The thermal resistance of a semiconductor device is generally defined as:

$$\theta_{JX} = \frac{T_J - T_X}{P_H}$$ Equation 1

where θ_{JX} = thermal resistance from device junction to a specific environment [°C/W]

T_J = device junction temperature in the steady state test condition [°C]

T_X = reference temperature for the specific environment [°C]

P_H = power dissipated in the device [W]

Common reference temperatures (X) are as follows:

T_A = reference temperature for the ambient environment, measured approximately three inches (7.62 cm) from the package

T_B = reference temperature for the board, measured on or near a ball or lead of the package

T_T = reference temperature for the top of the package, measured directly in the center, typically applicable for plastic packages

T_C = reference temperature for a package case, typically applicable for lidded or hermetic packages

Using experimental setups, one can empirically derive values of θ_{JX} for a variety of products and packages. For more detail, refer to the JESD51 standards Section 10, *References* on page 6.

4 Thermal Resistances and History

θ_{JA} is a value intended to represent the thermal resistance between the junction temperature and the ambient. Theoretically, if one had a correct value for θ_{JA} and the ambient temperature was known, the junction temperature could be computed with a straightforward calculation of *Equation 1* above. However, the conditions under which θ_{JA} is measured (see JESD51-2A) are often significantly different from actual use conditions in the application. In the test, the thermal test package is mounted to a PWB with no other surrounding packages or thermal influences, and the thermal parameters measured. The methodology for measuring θ_{JA} for hermetic and plastic packages is identical, and no significant problem presents itself in this instance. However, a great deal of confusion can arise when a user wishes to determine the junction temperature in an atypical situation or a situation where the user measures the package temperature themselves, and wishes to perform the computation based upon provided values of θ_{JC}.

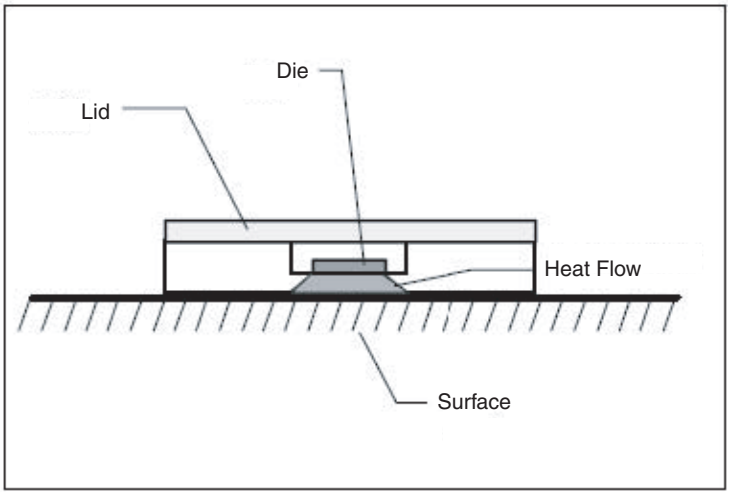
θ_{JC} is a measurement that is used to describe the internal thermal resistance of a packaged semiconductor device. Historically, the measurement was developed as a method of calculating junction temperature (T_J) from a known reference point on the outside of the package. The natural place for this reference point was defined as "the shortest thermal path from the junction to the outside of the package," which is also the best heat sinking surface. In the days when the specification for determining θ_{JC} was generated, the mainstream package was the ceramic DIP, which for the military, was mounted onto 'cold rails'; flat liquid cooled tubes that contacted the bottoms of the DIPS in the application. These cold rails were held at a constant temperature and served as a reference point for calculating T_J.

The test method is performed by bringing the desired package surface to thermal equilibrium, an isothermal case condition at some defined temperature, by using a large cold plate or heat sink. The purpose is to keep the external package temperature constant while the device is powered up. Heating voltage and current are supplied to the device to power up the die while keeping the package surface at the initial defined temperature. When the device comes to steady-state temperature and power conditions, the junction to case thermal resistance is calculated using *Equation 1*. The T_J is determined from the voltage and current output to the die, based upon a previously performed characterization of a thermal die, though such a characterization can be performed using a dynamic die (see JESD51-1).

5 Microelectronic Package Heat Flow

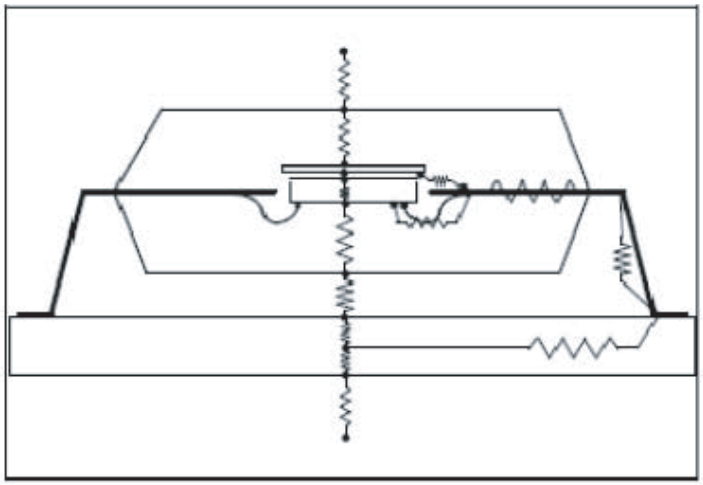
Heat flow in a hermetic package is well defined as illustrated in Figure 1. In the diagram it is seen that the die is attached to a ceramic substrate inside of a cavity. When the package is assembled, the cavity is left intact, that is, only air or some other gas comes in contact with the die surfaces not bonded to the cavity. Since the thermal conductivity of the ceramic is quite high when compared to air or other gasses, most of the heat gene rated (~90%) from the circuitry on the die surface is conducted through the silicon and into the ceramic substrate. The heat travels through the ceramic and is dissipated into the air or into a heat sink. Some spreading occurs in the ceramic (at an approximate 45° angle), so the analysis can be almost purely one-dimensional. This approach works well in any type of hermetic package including PGAs, CQFPs, CBGAs, and other ceramic packages.

Figure 1. Heat Flow in Hermetic Package



When plastic packages gained popularity, much of the thermal analysis was left intact, such as the θ_{JA} (junction-to-air thermal resistance parameter), and θ_{JC} (junction-to-case thermal resistance parameter). It was assumed, incorrectly, that the junction-to-case value could be used in plastic packages to predict junction temperature in the same way it was used for hermetic packages. The problem with θ_{JC} for plastic packages is fundamental, and it is easily seen how the physical construction of plastic packages negates the use of this simple parameter. Figure 2 shows the typical construction and heat flow in a plastic quad flat pack (PQFP). Heat flow paths are represented by a resistor network analogy in the diagram. As can be seen from the figure, heat flow in the plastic package is very complex when compared to the hermetic package. In plastic packages, the die is usually mounted onto a copper alloy die pad, wire bonded to the lead fingers which radially or orthogonally emanate from the die area, and is finally encapsulated in plastic molding compound. Because the die is contacted on all sides by solid matter, heat can flow easily in a multitude of directions. Due to the copper alloy's high thermal conductivity, the heat immediately spreads into the die attach paddle, and subsequently into the lead frame. Some heat also flows into the molding compound and is released by convection from the package external surfaces. BGA (Ball Grid Array) packages have a similar problem; heat is conducted directly away from the die through the metal traces and pathways within the substrate to the solder spheres and outside through the external surfaces of the package.

Figure 2. Heat Flow in Plastic Quad Flat Package



Through the years, the real identity of θ_{JC} was diluted, and today most system houses predict temperature by placing a thermocouple on the package surface and using the manufacturer's published θ_{JC} values to compute junction temperature. Unfortunately, it is an all too common practice and is accepted as correct. For plastic packages, there is no equivalent method for empirically computing a corresponding junction-to-case thermal resistance parameter.

6 Enter the Ψ_{JT} Parameter

In order to provide a more meaningful method to predict junction temperature in plastic packaged devices, the parameter Ψ_{JT} was created. This parameter, referenced in a number of JESD51 documents (specifically in JESD51-2A, from which most of the text below is derived) is proportional to the temperature difference between the top center of the package and the junction temperature. Hence, it is a useful value for an engineer verifying device temperatures in an actual environment. By measuring the package temperature of the device, the junction temperature can be estimated if the thermal characterization parameter has been measured under similar conditions. The use of Ψ_{JT} should not be confused with θ_{JC}.

The thermocouple bead is attached to the package at the geometric center of the top surface. The junction-to-top center of package thermal characterization parameter, Ψ_{JT}, is calculated using the following equation (assuming steady state conditions):

$$\Psi_{JT} = \frac{T_J - T_T}{P_H}$$ Equation 2

where Ψ_{JT} = thermal characterization parameter from device junction to package top [°C/W]

T_J = device junction temperature in the steady state test condition [°C]

T_T = the package (top surface) temperature, at steady-state [°C]

P_H = power dissipated in the device [W]

The relationship between the junction-to-ambient thermal resistance, θ_{JA}, and the junction-to-top center of package thermal characterization parameter, Ψ_{JT}, is described by:

$$\theta_{JA} = \Psi_{JT} + \Psi_{TA}$$ Equation 3

where Ψ_{TA} = thermal characterization parameter from top surface of the package-to-air [°C/W]

The package-to-air thermal characterization parameter, Ψ_{TA}, is based on the steady-state ambient air temperature as shown here:

$$\Psi_{TA} = \frac{T_T - T_A}{P_H}$$ Equation 4

The thermal characterization parameters, Ψ_{JT} and Ψ_{TA}, have the units °C/W but are mathematical constructs rather than thermal resistances because not all of the heating power flows through the exposed case surface. It is not necessary to compute Ψ_{TA} because it can be determined from the relationship between θ_{JA} and Ψ_{JT} which are measured as a typical part of experimental thermal analysis. Also, it should be noted that these thermal characterization values are very dependent on the application-specific environment.

7 Calculating T_J

As a matter of course, θ_{JA} and Ψ_{JT} values are provided in the reliability qualification summary for each particular product. In conditions described above (no significant localized heating, normal heat flow into the PWB), θ_{JA} values can be used in conjunction with the ambient temperature T_A to approximate the junction temperature, T_J. Ψ_{JT} can then be used to approximate the temperature of the top surface of the package. Alternatively, the temperature at the top surface of the package can be empirically measured and the Ψ_{JT} parameter can be used to approximate T_J. An example of an ideal case involving no localized heating is shown below in Figure 3. In this ideal case, a numerical computation using θ_{JA} should produce good correlation (*Equation 1*). This type of computation can also be performed where there are other packages in close proximity to the package in question. However, consider a situation with significant localized heating like that shown in Figure 4, where large dark packages representing the significant heat generators are placed close to the package. This heating will certainly impact the thermal gradient within the assembly and as a result, the numbers computed based upon the thermal correlation parameters may not be applicable. In a situation such as that in Figure 4, experiments ought to be performed in the application environment to determine the correct package thermal characterization parameters.

Figure 3. Ideal Conditions for Correlation

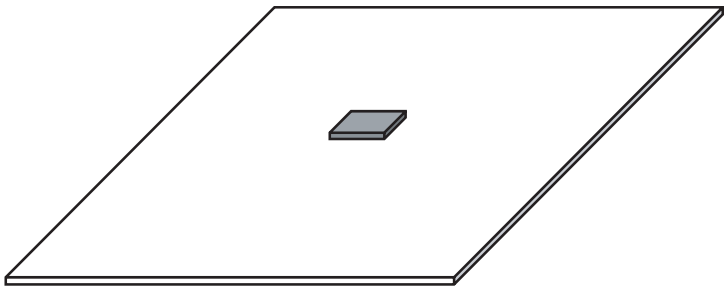
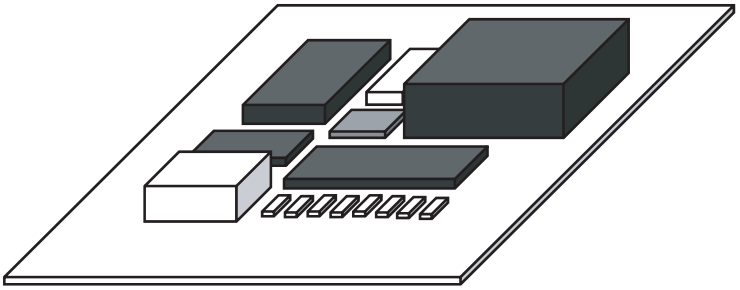


Figure 4. Atypical Conditions for Correlation



In order to better understand the mathematics behind this computation, an example calculation for the ideal case situation is presented below.

8 Calculating T_J in Ideal Conditions

Let us assume the conditions in Figure 3, with no localized heating. For a typical BGA package and product, the following are known:

θ_{JA} = 39°C/W

T_A = 55°C

P_H = 100 mW

Ψ_{JT} = 10.5°C/W

In this instance, the use of *Equation 1* gives us the following:

$$\theta_{JA} = \frac{T_J - T_A}{P_H}$$

Substituting the numbers, we have this equation:

$$39°C/\mathrm{W} = \frac{T_J - 55°C}{0.1W}$$

Solving for T_J gives us the following:

$$T_J = 39°C/\mathrm{W} \times 0.1W + 55°C$$
$$T_J = 58.9°C$$

As a result, we can easily compute the junction temperature, T_J, in this ideal case. If desired, using the Ψ_{JT} parameter, we can then use *Equation 2* to compute the package top temperature:

$$10.5°C/\mathrm{W} = \frac{58.9 - T_T°C}{0.1W}$$

Solving for T_T gives us the following:

$$T_T = 58.9°C - (10.5°C/\mathrm{W} \times 0.1W)$$
$$T_T = 57.9°C$$

Note that the measurement of T_A must be taken with care. If T_A is measured a great distance away from the package and there is some small localized heating due to an enclosure or other mechanism which prevents the ambient air from reaching the package, then the values computed will not be correct.

Additionally, as mentioned earlier, Ψ_{JT} can theoretically be used to compute T_J of a package in an assembly like that of Figure 4. However, because Ψ_{JT} was not characterized under similar conditions, such a computation should be performed with care.

9 Conclusion

This application note has attempted to clarify the origin and use of various thermal parameters and provide a straight forward methodology for computation of the junction temperature. By using these techniques and computations, a more accurate calculation of critical thermal temperatures can be made, and a better understanding of relevant thermal issues can be obtained.

10 References

- JESD51, Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Devices)
- JESD51-1, Integrated Circuit Thermal Measurement Method - Electrical Test Method
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-4, Thermal Test Chip Guideline (Wire Bond Type Chip)
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements
- AMD MSD Engineering Memo on Ψ_{JT}, Case Level Thermal Parameter

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	04/27/2011	Initial version
*A	5009313	MSWI	11/10/2015	Updated in Cypress template
*B	5724163	AESATP12	05/03/2017	Updated logo and copyright.
*C	6127034	BUHA	04/09/2018	Updated template
*D		MNAD	05/29/2019	Updated to SkyHigh format